## ABSTRACT

Depletion drain-extended MOS transistor devices and fabrication methods for making the same are provided, in which a compensated channel region is provided with p and n type dopants to facilitate depletion operation at Vgs = 0, and an adjust region is implanted in the substrate proximate the channel side end of the thick gate dielectric structure for improved breakdown voltage rating. The compensated channel region is formed by overlapping implants for an n-well and a p-well, and the adjust region is formed using a Vt adjust implant with a mask exposing the adjust region.